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<input type="checkbox"/>		L16	L15 and counter and ((edge or arc) near profil\$)	46
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<input type="checkbox"/>		L14	L13 or l1	4066
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<input type="checkbox"/>		L10	transition near phase	20914
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<input type="checkbox"/>		L9	profil\$ and (hardware near3 counter)	5
			<i>DB=USPT,PGPB; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>		L8	L5 and (counter near2 ID)	0
<input type="checkbox"/>		L7	L5 and (branch\$ near2 ID)	1
<input type="checkbox"/>		L6	L5 and (instruction near2 ID)	3
<input type="checkbox"/>		L5	L4 and edg\$	106
<input type="checkbox"/>		L4	profil\$ and (hardware near3 counter)	234
<input type="checkbox"/>		L3	L1 and profil\$ and (hardware near3 counter)	27
<input type="checkbox"/>		L2	L1 and profil\$ and counter	187
<input type="checkbox"/>		L1	((717/126 717/127 717/128 717/129 717/130 717/131 717/132 717/133 717/151 717/158)!.CCLS.)	1329

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Search Results - Record(s) 1 through 5 of 5 returned.

1. Document ID: JP 02310705 A

Using default format because multiple data bases are involved.

L9: Entry 1 of 5

File: JPAB

Dec 26, 1990

PUB-NO: JP402310705A

DOCUMENT-IDENTIFIER: JP 02310705 A

TITLE: RECONSTITUTABLE COUNTER AND ITS CONSTITUTION METHOD

PUBN-DATE: December 26, 1990

INVENTOR-INFORMATION:

NAME

COUNTRY

CRUICKSHANK, ANCIL B

DAVIS, RICHARD K

INT-CL (IPC): G05B 19/05

Full **Title** **Citation** **Front** **Review** **Classification** **Date** **Reference** **Claims** **KINIC** **Draw Desc** **In**

2. Document ID: NN76053935

L9: Entry 2 of 5

File: TDBD

May 1, 1976

TDB-ACC-NO: NN76053935

DISCLOSURE TITLE: Position Servo Utilizing Position Reference Clock. May 1976.

PUBLICATION-DATA:

IBM Technical Disclosure Bulletin, May 1976, US

VOLUME NUMBER: 18

ISSUE NUMBER: 12

PAGE NUMBER: 3935 - 3936

DISCLOSURE TEXT:

2p. The device and procedure described herein provides an implementation of a closed-loop servo system which can be made to follow some desired trajectory. - Fig. 1 is both an implementation of a hardware version and a microprocessor implementation. In Fig. 1, the circuits (shown in block diagram form) encircled by block 10 would be replaced by a microprocessor. Incidentally, block 10 is a representation of the microprocessor. - Fig. 2 is a sketch of the trajectory that the servo will follow. - The hardware

implementation that makes up the drive signal to motor 14 is comprised of reference voltage path A, which is an open-loop branch whose purpose is to apply a precalculated voltage profile to motor 14 via amplifier 12. If all system parameters are at their nominal values, the reference voltage derived from reference voltage path A would alone drive the system along the desired trajectories. Positional error path 13 is derived from the closed-loop portion of the servo system, and its magnitude is proportional to the difference between the position reference and the actual output position. - Referring to Fig. 1, the feedback signals on terminal 16 and terminal 18 are digital information derived from a two-phase digital tachometer 20. The problem therefore is to develop a digital signal $P_r(t)$ which is compatible with the digital system. - Fig. 3A shows a desired continuous output position trajectory denoted by $P_{do}(t)$. The vertical axis of the plot corresponds to position and has been divided into incremental position steps of Δ . Δ corresponds to the incremental position supplied by each cycle of the digital tachometer 20. Horizontal lines are drawn from each Δ on the vertical axis until the curve $P_{do}(t)$ is intersected. Another line is drawn vertically from the point of intersection to the horizontal axis which denotes time. - The sketch in Fig. 3B shows a train of pulses called Position Reference Clock which is derived from position reference clock generator 22. If the output of the servo did truly follow $P_{do}(t)$, then a full cycle of the digital tachometer would occur at each pulse location of the Position Reference Clock. Generation of the Position Reference Clock is then the desired reference, $P_r(t)$, for the closed-loop position servo system. - Generation of the position can be either done in hardware or by use of a microprocessor. A hardware version is shown in Fig. 4. Essentially the hardware version consists of a counter, reference crystal clock, some logic and a read-only memory. The memory contains the periods $T_1, T_2 \dots T_n$ of the tachometer 20 corresponding to desired output trajectory. The control logic sequentially loads in $T_1, T_2 \dots T_n$ from the memory into the down counter after each position reference pulse is generated. When the counter reaches zero, it puts out a pulse which is Position Reference Clock and a new T_n is loaded into the counter to continue the process. Incidentally, all hardware could be a portion of a microprocessor.

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Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstract	Claims	KM/C	Drawn Desc	C
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3. Document ID: US 6647491 B2, US 20020019930 A1

L9: Entry 3 of 5

File: DWPI

Nov 11, 2003

DERWENT-ACC-NO: 2002-216176

DERWENT-WEEK: 200382

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TITLE: Instruction profiling and trace selection system has hardware portion which detects more frequently executed instructions and software portion which forms trace of most frequently executed instructions

INVENTOR: BENITEZ, M; HSU, W C

PRIORITY-DATA: 1999US-0252567 (February 18, 1999), 2001US-0968283 (October 1, 2001)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<u>US 6647491 B2</u>	November 11, 2003		000	G06F015/00
<u>US 20020019930 A1</u>	February 14, 2002		009	G06F009/00

INT-CL (IPC): G06 F 9/00; G06 F 15/00

ABSTRACTED-PUB-NO: US20020019930A

BASIC-ABSTRACT:

NOVELTY - A hardware portion including counters and memory, detects which instructions of a program are more frequently executed and maintains a history of targets chosen by branch instructions of the program. A software portion forms the trace of the most frequently executed instructions and uses the maintained history in making branch predictions which are encountered in forming the trace.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for program instructions profiling method.

USE - For selecting profile instructions of a program and for selecting a trace of a portion of the instructions of the program.

ADVANTAGE - Uses the software which has more flexibility, less complexity and less expensive than hardware, for trace prediction and selection. Provides fast profiling and effective trace selection.

DESCRIPTION OF DRAWING(S) - The figure shows the trace selection mechanism.

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4. Document ID: DE 10194944 T, WO 200161499 A1, AU 200132543 A, US 20010021959 A1

L9: Entry 4 of 5

File: DWPI

Jun 12, 2003

DERWENT-ACC-NO: 2002-239485

DERWENT-WEEK: 200346

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TITLE: Processor system in computer, has hardware counters to measure performance characteristics of part entities of load module

INVENTOR: EGELAND, T; HOLMBERG, P A ; NORRMAN, P ; OESTEN, K ; JOHANSSON, L K ; JOHANSSON, L K O

PRIORITY-DATA: 2000SE-0000533 (February 18, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<u>DE 10194944 T</u>	June 12, 2003		000	G06F012/08
<u>WO 200161499 A1</u>	August 23, 2001	E	044	G06F012/08
<u>AU 200132543 A</u>	August 27, 2001		000	G06F012/08
<u>US 20010021959 A1</u>	September 13, 2001		000	G06F012/00

INT-CL (IPC): G06 F 12/00; G06 F 12/08

ABSTRACTED-PUB-NO: US20010021959A

BASIC-ABSTRACT:

NOVELTY - Memory allocation sections (38,41,48) is updated during a run time based on execution data provided by an execution profiling section (39). The profiling section has hardware counters (51) to measure performance characteristics of part entities of load modules (49,50) which has record and instruction data. Memory allocation section allocates selected part entities of load module to memory.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for memory handling method.

USE - In computer.

ADVANTAGE - More important data are held in static cache or the necessary memory size is reduced by a fine granularity of the data by the static cache. The access times are reduced due to close arrangement to the processor. Increases the flexibility by intermittently updating the allocation based on execution profile measurements.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of processor system.

Memory allocation sections 38,41,48

Execution profiling section 39

Load modules 49,50

Hardware counters 51

ABSTRACTED-PUB-NO:

WO 200161499A EQUIVALENT-ABSTRACTS:

NOVELTY - Memory allocation sections (38,41,48) is updated during a run time based on execution data provided by an execution profiling section (39). The profiling section has hardware counters (51) to measure performance characteristics of part entities of load modules (49,50) which has record and instruction data. Memory allocation section allocates selected part entities of load module to memory.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for memory handling method.

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DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of processor system.

Memory allocation sections 38,41,48

Execution profiling section 39

Load modules 49,50

Hardware counters 51

5. Document ID: SU 1105916 A

L9: Entry 5 of 5

File: DWPI

Jul 30, 1984

DERWENT-ACC-NO: 1985-060734

DERWENT-WEEK: 198510

COPYRIGHT 2004 DERWENT INFORMATION LTD

TITLE: Process control system moving hardware counter - has threshold forming signal triggering pulse generator at input to counter

INVENTOR: KOROTKOV, A V

PRIORITY-DATA: 1983SU-3590836 (May 10, 1983)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
SU 1105916 A	July 30, 1984		003	

INT-CL (IPC): G06M 7/00

ABSTRACTED-PUB-NO: SU 1105916A

BASIC-ABSTRACT:

Moving objects counter contg. the sensor (1), memory (5), comparator (7) and counter (8), has the threshold (2), pulse generator (3), counter (4) and the D/A converter (6).

As a detail passes through the sensor, the threshold forms a signal which triggers the pulse generator and so fills the counter. The memorised codes are obtained in quantising the data signal from the detail being registered. The memory presents consecutive codes which are converted into a stepped signal coinciding in shape with the signal from the detail. At coincidence the signal from the comparator is registered by the output counter.

USE/ADVANTAGE - In automatic counting of the output of automated process control systems, to identify details by the form of the sensor signal (the profile of the detail) as well as by the length of the detail, so increasing accuracy in differentiated counting of objects. Bul.28/30.7.84

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Terms	Documents
profil\$ and (hardware near3 counter)	5

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1 Ge/sub 2/Sb/sub 2/Te/sub 5/ thin film doped with silver [optical disc storage]

Lie, C.T.; Kuo, P.C.; Wu, T.H.; Chen, P.W.;
Optical Memory and Optical Data Storage Topical Meeting, 2002. International Symposium on, 7-11 July 2002
Pages:213 - 215

[\[Abstract\]](#) [\[PDF Full-Text \(227 KB\)\]](#) **IEEE CNF**

2 Measurement of the thermal coefficients of erasable phase-change media

Lu Cheng; Mansuripur, M.;
Optical Data Storage Topical Meeting, 1997. ODS. Conference Digest, 7-9 April 1997
Pages:96 - 97

[\[Abstract\]](#) [\[PDF Full-Text \(172 KB\)\]](#) **IEEE CNF**

3 Evaluation of force-sensing resistors for gait event detection to trigger electrical stimulation to improve walking in the child with cerebral palsy

Smith, B.T.; Coiro, D.J.; Finson, R.; Betz, R.R.; McCarthy, J.;
Neural Systems and Rehabilitation Engineering, IEEE Transactions on [see also IEEE Trans. on Rehabilitation Engineering], Volume: 10, Issue: 1, March 2002
Pages:22 - 29

[\[Abstract\]](#) [\[PDF Full-Text \(272 KB\)\]](#) **IEEE JNL**

4 Investigation of mechanical and antibiotic effects on TiN films deposited on medical tools by PACVD

Lee, H.; Park, S.S.; Kim, S.H.; Park, J.W.; Kim, D.J.; Lee, K.H.; Ahn, S.;

Plasma Science, 2002. ICOPS 2002. IEEE Conference Record - Abstracts. The 29th IEEE International Conference on , 26-30 May 2002
Pages:261

[\[Abstract\]](#) [\[PDF Full-Text \(178 KB\)\]](#) [IEEE CNF](#)

5 Vacuum packing: extracting hardware-detected program phases for post-link optimization

Barnes, R.D.; Nystrom, E.M.; Merten, M.C.; Hwu, W.W.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002
Pages:233 - 244

[\[Abstract\]](#) [\[PDF Full-Text \(686 KB\)\]](#) [IEEE CNF](#)

6 Time dependent electron deposition with thermal transport as applied to survivable anodes in flash X-ray machines

Rauch, J.E.;
Pulsed Power Conference, 1999. Digest of Technical Papers. 12th IEEE International , Volume: 2 , 27-30 June 1999
Pages:609 - 611 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(152 KB\)\]](#) [IEEE CNF](#)

7 Programmable frequency reference for laser stabilization using persistent spectral hole burning

Sellin, P.B.; Strickland, N.M.; Carlsen, J.L.; Cone, R.L.;
Lasers and Electro-Optics, 1999. CLEO '99. Summaries of Papers Presented at the Conference on , 23-28 May 1999
Pages:281 - 282

[\[Abstract\]](#) [\[PDF Full-Text \(212 KB\)\]](#) [IEEE CNF](#)

8 Femtosecond continuum generation using a gas-filled hollow fiber

Sokolowski-Tinten, K.; Werner, M.; Zhou, P.; Von Der Linde, D.;
Lasers and Electro-Optics, 1999. CLEO '99. Summaries of Papers Presented at the Conference on , 23-28 May 1999
Pages:324 - 325

[\[Abstract\]](#) [\[PDF Full-Text \(228 KB\)\]](#) [IEEE CNF](#)



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1 Phase tracking and prediction 99%

Timothy Sherwood , Suleyman Sair , Brad Calder

ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture May 2003

Volume 31 Issue 2

In a single second a modern processor can execute billions of instructions. Obtaining a bird's eye view of the behavior of a program at these speeds can be a difficult task when all that is available is cycle by cycle examination. In many programs, behavior is anything but steady state, and understanding the patterns of behavior, at run-time, can unlock a multitude of optimization opportunities. In this paper, we present a unified profiling architecture that can efficiently capture, classify, and ...

2 Profile-based optimizations: Dynamic trace selection using performance 97%

monitoring hardware sampling

Howard Chen , Wei-Chung Hsu , Jiwei Lu , Pen-Chung Yew , Dong-Yuan Chen

Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization March 2003

Optimizing programs at run-time provides opportunities to apply aggressive optimizations to programs based on information that was not available at compile time. At run time, programs can be adapted to better exploit architectural features, optimize the use of dynamic libraries, and simplify code based on run-time constants. Our profiling system provides a framework for collecting information required for performing run-time optimization. We sample the performance hardware registers available on ...

3 Software profiling for hot path prediction: less is more 93%

Evelyn Duesterwald , Vasanth Bala

Proceedings of the ninth international conference on Architectural support for programming languages and operating systems November 2000

Volume 34 , 28 Issue 5 , 5

Recently, there has been a growing interest in exploiting profile information in adaptive systems such as just-in-time compilers, dynamic optimizers and, binary translators. In this paper, we show that sophisticated software profiling schemes that provide highly accurate information in an offline setting are ill-suited for these dynamic code generation systems. We experimentally demonstrate that hot path predictions must be made early in order to control the rising cost of missed opportunity tha ...

4 Software profiling for hot path prediction: less is more

93%

 Evelyn Duesterwald , Vasanth Bala
ACM SIGPLAN Notices November 2000

Volume 35 Issue 11

Recently, there has been a growing interest in exploiting profile information in adaptive systems such as just-in-time compilers, dynamic optimizers and, binary translators. In this paper, we show that sophisticated software profiling schemes that provide highly accurate information in an offline setting are ill-suited for these dynamic code generation systems. We experimentally demonstrate that hot path predictions must be made early in order to control the rising cost of missed opportunity tha ...

5 Session 4B: multiagent resource allocation: Effort profiles in multi-agent

87%

 resource allocation

H. Van Dyke Parunak , Sven Brueckner , John Sauter , Robert Savit
Proceedings of the first international joint conference on Autonomous agents and multiagent systems: part 1 July 2002

Multi-agent systems are particularly appropriate for resource allocation, but configuring them for efficient operation requires understanding their dynamics. Concepts from statistical physics, such as phase transitions, can help. In decision problems such as constraint satisfaction, such transitions exhibit an easy-hard-easy effort profile, so that highly overconstrained problems are easier to solve than those near the transition. The conventional wisdom is that the profile in optimization probl ...

6 Positional adaptation of processors: application to energy reduction

85%

 Michael C. Huang , Jose Renau , Josep Torrellas
ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture May 2003

Volume 31 Issue 2

Although adaptive processors can exploit application variability to improve performance or save energy, effectively managing their adaptivity is challenging. To address this problem, we introduce a new approach to adaptivity: the *Positional* approach. In this approach, both the *testing* of configurations and the *application* of the chosen configurations are associated with particular code sections. This is in contrast to the currently-used *Temporal* approach to adaptation ...

7 The Performance of Runtime Data Cache Prefetching in a Dynamic

84%

 Optimization System

Jiwei Lu , Howard Chen , Rao Fu , Wei-Chung Hsu , Bobbie Othmer , Pen-Chung Yew , Dong-

Yuan Chen

Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture December 2003

Traditional software controlled data cache prefetching is often ineffective due to the lack of runtime cache miss and miss address information. To overcome this limitation, we implement runtime data cache prefetching in the dynamic optimization system ADORE (ADaptive Object code RE-optimization). Its performance has been compared with static software prefetching on the SPEC2000 benchmarksuite. Runtime cache prefetching shows better performance. On

- an Itanium 2 based Linux workstation, it can increase ...

8 Temperature and power aware architectures: Routine based OS-aware microprocessor resource adaptation for run-time operating system power saving 83%
 Tao Li , Lizy Kurian John
Proceedings of the 2003 international symposium on Low power electronics and design August 2003
The increasingly constrained power budget of today's microprocessor has resulted in a situation where power savings of all components in a system have to be taken into consideration. Operating System (OS) is a major power consumer in many modern applications execution. This paper advocates a routine based OS-aware microprocessor resource adaptation mechanism targeting run-time OS power savings. Simulation results show that compared with the existing sampling-based adaptation schemes, this novel ...

9 Physically based modeling and animation of fire 82%
 Duc Quang Nguyen , Ronald Fedkiw , Henrik Wann Jensen
ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual conference on Computer graphics and interactive techniques July 2002
Volume 21 Issue 3
We present a physically based method for modeling and animating fire. Our method is suitable for both smooth (laminar) and turbulent flames, and it can be used to animate the burning of either solid or gas fuels. We use the incompressible Navier-Stokes equations to independently model both vaporized fuel and hot gaseous products. We develop a physically based model for the expansion that takes place when a vaporized fuel reacts to form hot gaseous products, and a related model for the similar ex ...

10 Modeling waves and surf 82%
 Darwyn R. Peachey
ACM SIGGRAPH Computer Graphics , Proceedings of the 13th annual conference on Computer graphics and interactive techniques August 1986
Volume 20 Issue 4

11 Accurate indirect branch prediction 80%
 Karel Driesen , Urs Hözle
ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture April 1998
Volume 26 Issue 3
Indirect branch prediction is likely to become increasingly important in the future because indirect branches occur more frequently in object-oriented programs. With misprediction rates of around 25% on current processors, indirect branches can incur a significant fraction of branch misprediction overhead even though they remain less frequent than the more predictable conditional branches. We investigate a wide range of two-level predictors dedicated exclusively to indirect branches. Starting wi ...

12 Military applications: Winter simulation: development of a fast all-seasons model for the state of the ground 80%
 Mary Albert , George Koenig , George Mason
Proceedings of the 32nd conference on Winter simulation December 2000
For predicting soil conditions in support of mobility, combat, or engineering simulations, it is important to have verified models that can reliably predict the state of the ground in all weather conditions. While variations in the state of the ground in summer are due primarily

to soil type, vegetation, and slope, the winter and spring seasons present additional challenges that are currently not addressed by most Army models. Because the depth of snow on the ground varies greatly through the wi ...

13 Simulation of a local area network for a newspaper production system 80%

 J. Agre , I. Shahnaz , M. Atkinson , D. Joshi , A. A. R. K. Sastry

Proceedings of the 19th conference on Winter simulation December 1987

A computer simulation model has been developed for a Local Area Network (LAN)-based newspaper production system (NPS). The objective is to develop a model that serves as a performance evaluation and design tool for the NPS operation in a Manufacturing Automation Protocol (MAP) environment. The approach taken involved developing three modules that mimic the seven layers of the MAP/OSI (Open System Interconnection) model from a performance evaluation perspective: (1) the medium access module ...

14 Dynamically allocating processor resources between nearby and distant ILP 77%

 Rajeev Balasubramonian , Sandhya Dwarkadas , David H. Albonesi

ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture May 2001

Volume 29 Issue 2

Modern superscalar processors use wide instruction issue widths and out-of-order execution in order to increase instruction-level parallelism (ILP). Because instructions must be committed in order so as to guarantee precise exceptions, increasing ILP implies increasing the sizes of structures such as the register file, issue queue, and reorder buffer.

Simultaneously, cycle time constraints limit the sizes of these structures, resulting in conflicting design requirements.

In ...

15 Runtime Power Monitoring in High-End Processors: Methodology and 77%

 Empirical Data

Canturk Isci , Margaret Martonosi

Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture December 2003

With power dissipation becoming an increasingly vexing problem across many classes of computer systems, measuring power dissipation of real, running systems has become crucial for hardware and software system research and design. Live power measurements are imperative for studies requiring execution times too long for simulation, such as thermal analysis. Furthermore, as processors become more complex and include a host of aggressive dynamic power management techniques, per-component estimates of power ...

16 Generational Cache Management of Code Traces in Dynamic Optimization 77%

 Systems

Kim Hazelwood , Michael D. Smith

Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture December 2003

A dynamic optimizer is a runtime software system that groups a program's instruction sequences into traces, optimizes those traces, stores the optimized traces in a software-based code cache, and then executes the optimized code in the code cache. To maximize performance, the vast majority of the program's execution should occur in the code cache and not in the different aspects of the dynamic optimization system. In the past, designers of dynamic optimizers have used the SPEC2000 benchmark suite to just ...

17 Modeling and manipulation: Volumetric ablation rendering

77%

 Hari Varadhan , Klaus Mueller**Proceedings of the 2003 Eurographics/IEEE TVCG Workshop on Volume graphics** July 2003

In this paper, we propose a physically-based method for simulating the process of ablation on volumetric models. We demonstrate the visual effect of ablative processes, such as a beam of heat emitted from a blow torch or a pencil of sand expelled from a sandblaster. Users are able to control ablative properties, such as energy propagation, absorption, and material evaporation, via a simple transfer function interface, while the effect of different beam shapes can be modeled by ways of weighting ...

18 The heuristic synthesis of applications-oriented microcode

77%

 A. M. Abdalla , D. C. Karlgaard**Conference record of the 6th annual workshop on Microprogramming** September 1973

This paper describes an algorithm for the synthesis of applications-oriented microcode for a dynamically microprogrammable computer. The need for such an algorithm is expressed by Reigel, Faber, and Fisher as an integral step in the solution of the tuning problem, or the problem of modifying a system architecture in order to optimally solve a given problem. This modification of architecture takes place through synthesis of microprograms that are stored in writable control storage. Writable ...

19 Run-time modeling and estimation of operating system power consumption

77%

 Tao Li , Lizy Kurian John**ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2003 ACM SIGMETRICS international conference on Measurement and modeling of computer systems** June 2003

Volume 31 Issue 1

The increasing constraints on power consumption in many computing systems point to the need for power modeling and estimation for all components of a system. The Operating System (OS) constitutes a major software component and dissipates a significant portion of total power in many modern application executions. Therefore, modeling OS power is imperative for accurate software power evaluation, as well as power management (e.g. dynamic thermal control and equal energy scheduling) in the light of ...

20 Dynamic Adaptive compilation: Dynamic profiling and trace cache generation

77%

 Marc Berndl , Laurie Hendren**Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization** March 2003

Dynamic program optimization is increasingly important for achieving good runtime performance. A key issue is how to select which code to optimize. One approach is to dynamically detect traces, long sequences of instructions spanning multiple methods, which are likely to execute to completion. Traces are easy to optimize and have been shown to be a good unit for optimization. This paper reports on a new approach for dynamically detecting, creating and storing traces in a Java virtual machine. We ...

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15% Off List Prices ... around Bridges' 3-phase transition model of endings, the ...
www.internalchange.com/disc_profile_store/mall/ProductPage10.asp

2. Biophysical Journal – Lasch et al. 75 (2): 840

... This figure shows a typical (T) phase transition profile obtained for the DMPEd54 component in a binary ... pronounced and even sharper phase transition profile than that observed for the ...
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www.agri.gov.il/AnimalScience/Reproduction/Rep-Arv2.html - 3k - Cached

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Diffusion, Segregation and Stresses in Materials published in Defect and Diffusion Forum. ... the depth of the energetic profile for the dense packed CSL planes ...
www.ttp.net/3-908450-76-4/93.htm - 10k - Cached

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Straub, J.; Lange, R.; Nitsche, K.; **Phase transition;TEXUS 8** ...
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www.esrin.esa.it/mgdb/european_experiments/mgdb444f4336d12b990e.html

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... chainon the **phase transition** behavior of lipid bilayers ... **crystalline phase transition** temperature. Specifically, in the plot of T_m versus n , an inverted bell-shaped profile is ...
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19. [**Transition - ThePersonal Path Through Change - Empowerment-Plus.com**](#) 

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